

10 the first amount of data corresponding to the first block size  
11 information; and

12 providing a first portion of the first amount of data to the  
13 memory device synchronously with respect to a first transition of  
14 an external clock signal, and a second portion of the first  
15 amount of data synchronously with respect to a second transition  
16 of the external clock signal.

*a2 cont.*  
1 <sup>2</sup>/<sub>152</sub>. The method of claim <sup>1</sup>/<sub>151</sub> further including providing a  
2 second block size information to the memory device wherein the  
3 second block size information defines a second amount of data to  
4 be input by the memory device in response to a second write  
5 request.

<sup>3</sup>/<sub>153</sub>. The method of claim <sup>1</sup>/<sub>151</sub> further including:  
issuing a second write request to the memory device, wherein  
in response to the second write request the memory device samples  
a second amount of data corresponding to second block size  
information; and

6 providing a first portion of the second amount of data to  
7 the memory device synchronously with respect to a third  
8 transition of the external clock signal, and a second portion of  
9 the second amount of data synchronously with respect to a fourth  
10 transition of the external clock signal.





1 <sup>14</sup>  
~~164.~~ The method of claim <sup>13</sup>  
~~163~~ wherein the first transition  
2 of the external clock signal is a rising edge transition and the  
3 second transition of the external clock signal is a falling edge  
4 transition.

1 <sup>15</sup>  
~~165.~~ The method of claim <sup>13</sup>  
~~163~~ further including receiving  
2 second block size information from the master, wherein the second  
3 block size information defines a second amount of data to be  
4 input by the memory device in response to a second write request.

1 <sup>16</sup>  
~~166.~~ The method of claim <sup>13</sup>  
~~163~~ further including:  
2 receiving a second write request from the master; and  
3 inputting a second amount of data corresponding to second  
4 block size information synchronously with respect to a third  
5 transition of the external clock signal and a second portion of  
6 the first amount of data synchronously with respect to a fourth  
7 transition of the external clock signal.

1 <sup>17</sup>  
~~167.~~ The method of claim <sup>16</sup>  
~~166~~ wherein the third and fourth  
2 transitions of the external clock cycle transpire during a common  
3 clock cycle of the external clock signal.

1 <sup>18</sup>  
~~168.~~ The method of claim <sup>13</sup>  
~~163~~ wherein the first block size  
2 information and the first write request are included in the same  
3 request packet.

1 <sup>19</sup>  
~~169.~~ The method of claim <sup>13</sup>  
~~163~~ wherein the first block size  
2 information is a binary representation of the first amount of  
3 data to be input in response to the first write request.

1 <sup>20</sup>~~170~~. The method of claim <sup>13</sup>~~163~~ wherein the first amount of  
2 data corresponding to the first block size information is input  
3 synchronously during <sup>the same</sup>~~one~~ clock cycle of the external clock  
4 signal.

1 <sup>21</sup>~~171~~. The method of claim <sup>13</sup>~~163~~ wherein the first amount of  
2 data corresponding to the first block size information is sampled  
3 synchronously during a plurality of clock cycles of the external  
4 clock signal.

1 <sup>22</sup>~~172~~. The method of claim <sup>13</sup>~~163~~ further including generating  
2 an internal clock signal using a delay locked loop circuit and  
3 the external clock signal wherein the first amount of data  
4 corresponding to the first block size information is sampled in  
5 response to the internal clock signal.

1 <sup>23</sup>~~173~~. The method of claim <sup>13</sup>~~163~~ further including generating  
2 first and second internal clock signals using clock generation  
3 circuitry and the external clock signal wherein the first amount  
4 of data corresponding to the first block size information is  
5 sampled synchronously with respect to the first and second  
6 internal clock signals.

1 <sup>24</sup>~~174~~. A method of operation of an integrated circuit device  
2 having a synchronous interface, the method of operation of the  
3 integrated circuit device comprising:

4 receiving block size information, wherein the block size  
5 information defines an amount of data to be sampled by the  
6 integrated circuit device in response to a write request;

7 receiving a write request; and

8 sampling a first portion of the amount of data synchronously  
9 with respect to a first transition of an external clock signal  
10 and a second portion of the amount of data synchronously with  
11 respect to a second transition of the external clock signal,  
12 wherein the first and second transitions of the external clock  
13 signal <sup>occur</sup> ~~transpire~~ during <sup>the same</sup> ~~one~~ clock cycle of the external clock  
14 signal.

*25*  
~~175~~. The method of claim *24* ~~174~~ wherein the first transition  
of the external clock signal is a rising edge transition and the  
second transition of the external clock signal is a falling edge  
transition.

*26*  
~~176~~. The method of claim *24* ~~174~~ further including:  
receiving a read request; and

outputting a first portion of the amount of data  
synchronously with respect to a third transition of the external  
clock signal and a second portion of the amount of data  
synchronously with respect to a fourth transition of the external  
clock signal.

1 <sup>27</sup>/~~177~~. The method of claim <sup>24</sup>/~~174~~ wherein the block size  
2 information and the write request are included in the same  
3 request packet.

1 <sup>28</sup>/~~178~~. The method of claim <sup>24</sup>/~~174~~ wherein the block size  
2 information is a binary representation of the amount of data to  
3 be sampled in response to the write request.

1 <sup>29</sup>/~~179~~. The method of claim <sup>24</sup>/~~174~~ further including generating  
2 an internal clock signal using a delay locked loop and the  
3 external clock signal wherein the amount of data corresponding to  
4 the block size information is input synchronously with respect to  
5 the internal clock signal. --

**REMARKS**

This Preliminary Amendment seeks to place this application in condition for allowance. This application is a continuation of Application Serial No. 09/252,998, which is a continuation of Application Serial No. 08/979,127, now U.S. Patent 5,915,105. Application Serial No. 09/252,998 is still pending.

Applicants request priority to Application Serial No. 07/510,898, filed April 18, 1990, now abandoned. Applicants request such priority through Application No. 09/252,998, filed on February 19, 1999 (still pending), which is a continuation of Application No. 08/979,127, filed on November 26, 1997 (now U.S. Patent 5,915,105), which is a continuation of Application No.